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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/212,291	12/16/98	PRUDVI C	2207/5915

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KENYON & KENYON
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WASHINGTON DC 20005

EXAMINER	
THAI, T	
ART UNIT	**PAPER NUMBER**
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Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No. 09/212,291	Applicant(s) PRUDVI ET AL.	
	Examiner Tuan V. Thai	Art Unit 2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 July 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

Part III DETAILED ACTION

Response to Amendment

1. This office action is in response to Applicant's communication filed May 16, 2001. This amendment has been entered and carefully considered. Claims 1-20 remain pending in the application.

2. Applicant's arguments with respect to claims 1-20 have been considered but are deemed to be moot in view of the new grounds of rejection. The finality of the previous office action is hereby withdrawn. Any inconvenience is *SINCERELY* regretted.

3. Drawing 1 is objected to since the Bus Sequencing Unit 200 (BSU) being mentioned on page 3, line 23 of the specification can not be cited in Figure 1. Correction is required.

Claim Rejections - 35 USC § 112

4. As per claim 6, the recitations of "the status information" (line 1), and "the first external transaction" (lines 1-2) lack proper antecedent basis. It appears that claim 6 should be dependent on claim 5. Correction is required.

As per claim 7, the recitations of "the total number of primary and secondary entries" (line 1) and "the multiple number of data line lengths" (line 2) lacks proper antecedent basis. It appears that claim 6 should be dependent on claim 5. Correction is required.

Claim Rejections - 35 USC § 102

55. The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 8-10 and 22 are rejected under 35 U.S.C. 102(b) as being anticipated by Sachs et al. (USPN: 4,884,197) (hereinafter Sachs).

As per claim 8, Sachs teaches the invention as claimed including a processing agent comprising a transaction queue as being equivalent to the TLB 350 having a plurality of queue entries (lines) (e.g. see column 22, line 49 et seq.), wherein the queue entries further comprising a primary sub entry including an address information and status information provided for a first external transaction, and a secondary subentry provided including a status portion provided for a second external transaction is explicitly taught by Sachs as each line

having virtual address field VA for storing address information and a reference bit R field or a dirty bit D field for storing status information of the first external transaction being read/write transactions (with respect to the status for the second external transaction, note also an user valid bit UV field, a superior valid bit field, a protection level word PL field and a system tag ST field; e.g. see column 22, lines 59 et seq.; column 24, lines 27 et seq.);

As per claim 9, wherein the status portion of the primary entry includes a field representing whether the first transaction is part of a multiple transaction queue is equivalently taught by Sachs as the reference bit R or the dirty bit D field of each line indicating that the line has been referenced by a read or write transaction (multiple transaction sequence), or having been modified by a write transactions (e.g. see column 22, lines 59 et seq.; column 24, lines 27 et seq.);

As per claim 10, Sachs discloses the TLB control logic unit 820 as being equivalent to the control logic being claimed, coupling to the TLB 350 for cycle through the queue entries and post transaction therefrom (e.g. see figure 23);

As per claim 22, see argument with respect to claim 8.

4. Claims 17-21 and 23 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Sachs (USPN: 4,884,197), and being

anticipated by Scales et al. (USPN: 4,914,573) (hereinafter Scales).

As per claims 17 and 18, Scales discloses the invention as claimed including a method of processing a data request within a processing agent comprising posting the data request internally within the agent, determining whether the cache hit by comparing address information of the data request with tags stored in the internal cache, and if cache miss occurs, posting a sequence of external transactions to fill a cache line with data associated with the data request (e.g. see column 1, lines 12-32);

As per claim 19; reading the cache coherency state information associated with the requested data when address information matches a stored tag, and identifying cache miss when coherency information is invalid is embedded in Scales's system and being taught to the extent that it is claimed, since Scales discloses in a conventional system the cache are arranged as a plurality of lines, each containing plurality of entries which share a common "tag address", ***and a corresponding number of valid bits which when set indicate the validity of the respective entries in the particular cache line*** (e.g. see Scales's column 1, lines 12-17);

As per claims 20 and 21; Scales teaches the determining whether the request hits a tag stored in the cache by comparing the requested data address information with a tag address and

generating a single transaction to read the requested data into the agent (e.g. see column 1, lines 19-21;);

As per claim 23, Scales discloses the invention as claimed including a method of processing a data request within a processing agent comprising posting the data request internally within the agent, determining whether the request hit in the cache, when cache miss occurs, posting a series of external transaction to fill a cache line with data associated with the data request (e.g. see column 1, lines 12-32); the external transactions directed to a data-line sized data item identified by an address of the data request and to at least one other data-line-sized item adjacent to the first data item (e.g. see column 2, lines 55-66).

Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-7 and 11-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sachs et al. (USPN: 4,884,197); hereinafter Sachs, in view of Scales, III et al., (USPN:

4,914,573) (hereinafter Scales).

As per claim 1, Sachs teaches the invention as claimed including a processing agent (e.g. see figures 8 and 9) to transfer data of predetermined data length in an external transaction, the agent comprising an cache memory 320 having a plurality of cache entries; for example, Sachs discloses that the cache memory 320 having three fields, a used bit field, and two identical read-write memory fields W and X wherein each field W and X contain multiple lines, and each line in the cache contains multiple entries (fields) (e.g. see figure 10.B) and having tag field RA, line valid bit LV, line dirty bit LD and multiple data entries DT (e.g. see column 22, lines 14 et seq.). Sachs discloses the invention as claimed; however Sachs does not particularly teach that each entry sized to store multiple data line lengths of data. Scales, in his teaching of bus master which selectively attempts to fill complete entries in a cache line, disclose the missing element that known to be required in Sachs in order to arrive at Applicant's current invention wherein Sachs teaches cache memory 22 having a plurality of cache entries (e.g. see column 2, lines 38 et seq.), each of the cache entries include a tag portion for storing address information RA (e.g. see figure 2, column 2, lines 38 et seq.), cache coherency state field [A3, A2] wherein each entry can be sized to store multiple data line lengths of data (e.g. see column 7, lines 59 et seq.).

Accordingly, it would have been obvious to one having ordinary skill in the art at the time the current invention was made to implement the cache having multiple cache lines comprising multiple entries, wherein each entry sized to store multiple data line lengths of data as being taught by Scales for that of Sachs. In doing so, it would increase the flexibility of Sachs system by allowing it to serve a broader range of applications and their variants thereby broadening one's potential market and saving investment capital.

As per claim 2, Sachs clearly discloses that the cache entries include a tag portion for storing address information as being the real address field RA (e.g. see figure 10B, and column 22, lines 32 et seq.);

As per claim 3, the match detection logic for the tag portions and control logic provided in communication with the match detection logic is taught by Sachs as the comparators 332 and 334, and the multiplexer 341 (e.g. see figure 9, column 21, lines 4 et seq.; for example, Sachs discloses the match/no match signals output from comparators 332 and 334 indicate a cache hit when the requested real address was presented in the cache and the data was valid, or a cache miss when the requested data is not present in the cache (e.g. see column 21, lines 20 et seq.);

As per claim 4, Sachs clearly teaches each cache line further have a cache coherency state field such that: a cache

line valid bit LV, a line dirty bit DT (e.g. see figure 10B, column 22, lines 28 et seq.);

As per claim 5, Sachs discloses his processing agent further comprising a transaction queue as being equivalent to the TLB 350 having a plurality of queue entries (lines) (e.g. see column 22, line 54 et seq.), wherein the queue entries including a primary entry for storing address information and status information of a first external transaction, and a secondary entry for storing status information of a second external transaction is explicitly taught by Sachs as each line having virtual address field VA for storing address information and a reference bit R field or a dirty bit D field for storing status information of an external transaction being read/write transactions (note also an user valid bit UV field, a superior valid bit field, a protection level word PL field and a system tag ST field; e.g. see column 22, lines 59 et seq.; column 24, lines 27 et seq.);

As per claim 6, wherein the status information of the first external transaction includes a field (e.g. the reference bit R or the dirty bit D) indicating that the line has been referenced by a read or write transaction (multiple transaction sequence), or having been modified by a write transactions (e.g. see column 22, lines 59 et seq.; column 24, lines 27 et seq.);

As per claim 7, Sachs discloses the invention as claimed; however Sachs does not particularly teach that the total number

of primary and secondary entries equals to the number of data line lengths provided in the cache entries. First of all, it should be noted that the total number of lines in both cache and TLB being disclosed in Sachs's system is a system dependent feature, it can be varied dependent on what system they are implemented within. Secondly, Sachs clearly discloses the W and X memories in BOTH cache memory 320 and TLB 350 each contain multiple lines, and as an example for illustration in the current invention, Sachs selects the number of cache lines being equal to 128 lines (e.g. see column 22, line 22); and the number of lines in the TLB is 64 lines (e.g. see column 22, line 54). Accordingly, it would have been obvious to one having ordinary skill in the art at the time the current invention was made to implement both cache and TLB to have the same number of lines since the numbers of lines in both cache and TLB are changeable as indicated by Sachs. In addition, doing so, it would allow the TLB to buffer more data for reference which results to increasing data hit rate in both TLB and cache, therefore being advantageous.

As per claim 11, Sachs disclose a processing agent (e.g. see figures 8 and 9) comprising an cache memory 320 having a plurality of cache entries; for example, Sachs discloses that the cache memory 320 having three fields, a used bit field, and two identical read-write memory fields W and X wherein each field W

and X contain multiple lines, and each line in the cache contains multiple entries (fields) (e.g. see figure 10.B) and having tag field RA, line valid bit LV, line dirty bit LD and multiple data entries DT (e.g. see column 22, lines 14 et seq.). A transaction queue system as being equivalent to the TLB 350 having a plurality of queue entries (lines) to post external transactions, each external transaction related to a single data line (e.g. see column 22, line 54 et seq.), wherein the internal cache and the transaction queue system each receive data requests on a common input (e.g. see figure 8 show common input line being connected to both TLB 270 and cache 220). Sachs discloses the invention as claimed; however Sachs does not particularly teach that each entry sized to store multiple data line lengths of data. Scales, in his teaching of bus master which selectively attempts to fill complete entries in a cache line, disclose the missing element that known to be required in Sachs in order to arrive at Applicant's current invention wherein Sachs teaches cache memory 22 having a plurality of cache entries (e.g. see column 2, lines 38 et seq.), each of the cache entries include a tag portion for storing address information RA (e.g. see figure 2, column 2, lines 38 et seq.), cache coherency state field [A3, A2] wherein each entry can be sized to store multiple data line lengths of data (e.g. see column 7, lines 59 et seq.). Accordingly, it would have been obvious to one having ordinary skill in the art

at the time the current invention was made to implement the cache having multiple cache lines comprising multiple entries, wherein each entry sized to store multiple data line lengths of data as being taught by Scales for that of Sachs. In doing so, it would increase the flexibility of Sachs system by allowing it to serve a broader range of applications and their variants thereby broadening one's potential market and saving investment capital.

As per claim 12, wherein the internal cache and the transaction queue system communicate by signal lines (e.g. see figure 8);

As per claim 13, wherein the signals line include a cache hit signal line and a tag hit signal line (e.g. see figure 9, column 19, lines 58 et seq.; column 20, lines 4 et seq.);

As per claim 14, Sachs teaches the invention as claimed including a processing agent comprising a transaction queue as being equivalent to the TLB 350 having a plurality of queue entries (lines) (e.g. see column 22, line 54 et seq.), wherein the queue entries further comprising a primary sub entry including an address information and status information provided for a first external transaction, and a secondary subentry provided including a status portion provided for a second external transaction is explicitly taught by Sachs as each line having virtual address field VA for storing address information and a reference bit R field or a dirty bit D field for storing

status information of first external transaction being read/write transactions (with respect to status for the second external transaction, note also an user valid bit UV field, a superior valid bit field, a protection level word PL field and a system tag ST field; e.g. see column 22, lines 59 et seq.; column 24, lines 27 et seq.);

As per claim 15, wherein the status portion of the primary entry includes a field representing whether the first transaction is part of a multiple transaction queue is equivalently taught by Sachs as the reference bit R or the dirty bit D field of each line indicating that the line has been referenced by a read or write transaction (multiple transaction sequence), or having been modified by a write transactions (e.g. see column 22, lines 59 et seq.; column 24, lines 27 et seq.);

As per claim 16, Sachs discloses the TLB control logic unit 820 as being equivalent to the control logic being claimed, coupling to the TLB 350 for cycle through the queue entries and post transaction therefrom (e.g. see figure 23);

10. Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

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or faxed to:

(703) 308-9051 (for formal communications intended for

entry)

Or:

(703) 308-6606 (for informal or draft communications, please label "PROPOSED" or "DRAFT")
Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA., Sixth Floor (Receptionist).

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan V. Thai whose telephone number is 703-305-3842.

The examiner can normally be reached on Monday-Thursday from 6:30 AM to 4:00 PM. The examiner can also be reached on alternate Fridays or e-mailed at ***tuan.thai@uspto.gov;***

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor Matthew M. Kim can be reached on (703) 305-3821.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-3900. The Official Fax Numbers for TC-2100 are:

After-final	***(703) 746-7238***
Official	***(703) 746-7239***
Non-Official/Draft	***(703) 746-7240***

TVT/October 17, 2001

Tuan V. Thai

PRIMARY EXAMINER

Group 2100